IN THE CLAIMS:

Please amend claims 1, 12, 15, 18 and 20, and add new claims 22-25 as follows:

Claim 1. (currently amended) A decoding circuit comprising:

an input unit for entering coded digital signals in parallel in accordance with a number of interleaved codes;

a ~~processor, said~~ processor ~~in turn~~ comprising an error locator polynomial calculator and an error value polynomial calculator, for processing data obtained serially from said interleaved codes that are received by said input unit; ~~and~~

an output unit for correcting errors by employing output data that is received serially from said processor and said digital signals, and for outputting ~~the~~ obtained digital signals in parallel in accordance with said number of interleaved codes; and

wherein the processor comprises a three stage multiplier, the three stage multiplier including an input side XOR calculator group, an AND calculator group, and an output side calculator group.

Claim 2. (original) The decoding circuit according to claim 1, wherein said input unit calculates syndromes for said input digital signals, and transmits said syndromes for interleaved codes to said processor serially;

wherein said processor employs said syndromes to calculate coefficients of an error locator polynomial and coefficients of an error value polynomial; and

wherein said output unit, based on said coefficients of said error locator polynomial and said coefficients of said error value polynomial received from said processor, generates error locations and error values, using a linear calculation in a Galois extension field for said input digital signals, and defines said error locations and said error values as said digital signals to be output.

Claim 3. (original) The decoding circuit according to claim 1, wherein said input digital signals are Reed-Solomon codes that are received in parallel through an i-channel, and the decoding circuit comprises at least one of a multiplexer and a demultiplexer, having a ratio of one of i:1 and 1:i.

Claim 4. (original) The decoding circuit according to claim 1, wherein, for optical communication, wavelength division multiplexing is used for the transmission of said input digital signals.

Claim 5. (original) The decoding circuit according to claim 1, wherein said input unit comprises a sequential circuit and said processor comprises a combinational circuit.

Claim 6. (original) The decoding circuit according to claim 1 that is used for at least one of the correction of digital signal errors and encryption.

Claim 7. (currently amended) A decoder comprising:

input means, for receiving coded digital signals;

processing means, for processing said coded digital signals and for calculating coefficients of an error locator polynomial and coefficients of an error value polynomial; and

output means, for outputting digital signals for which errors have been corrected using said coefficients of said error locator polynomial and said coefficients of error value polynomial,

wherein said input means receives in parallel, in accordance with a number of interleaved codes, said coded digital signals, and employs said coded digital signals to calculate syndromes as data obtained serially from said interleaved codes,

wherein said processing means employs said syndromes output by said processing means to calculate said coefficients of said error locator polynomial and said coefficients of said error value polynomial, and

wherein said output means employs said coefficients of said error locator polynomial, said coefficients of said error value polynomial and said coded input digital signals to correct errors using a linear calculation in a Galois extension field, and outputs in parallel ~~the~~ obtained digital signals in accordance with said number of interleaved codes; and

wherein the processing means comprises a three stage multiplier, the three stage multiplier including an input side XOR calculator group, an AND calculator group, and an output side calculator group.

Claim 8. (original) The decoder according to claim 7, wherein said input digital signals are Reed-Solomon codes that are received in parallel through an i-channel, and the decoder comprises at least one of a multiplexer and a demultiplexer having a ratio of one of i:1 or 1:i.

Claim 9. (original) The decoder according to claim 7, wherein, for optical communication, wavelength division multiplexing is used for transmission of said input digital signals.

Claim 10. (original) The decoder according to claim 7, wherein said input unit comprises a sequential circuit and said processor comprises a combinational circuit.

Claim 11. (original) The decoder according to claim 7 that is used for at least one of the correction of digital signal errors and encryption.

Claim 12. (currently amended) A method for decoding a digital signal comprising:

an input step of entering coded digital signals in parallel in accordance with a number of interleaved codes;

a process step of employing a processor, including an error locator polynomial calculator and an error value polynomial calculator, to process data obtained serially from said interleaved codes that are received at said input unit;

a generation step of employing said output data that is received from said processor and said digital signals to generate digital signals for which an error has been corrected; and

an output step of outputting ~~the~~ obtained digital signals in parallel in accordance with said number of interleaved codes; and

employing a three stage multiplier, the three stage multiplier including an input side XOR calculator group, an AND calculator group, and an output side calculator group.

Claim 13. (original) The decoding method according to claim 12, wherein said input step includes the step of:

calculating syndromes for said input digital signals, and transmitting said syndromes to said processor as data obtained serially from interleaved codes,

wherein said process step includes the step of:

employing said syndromes to calculate coefficients of an error locator polynomial and coefficients of an error value polynomial, and

wherein said output step includes the step of:

based on said coefficients of said error locator polynomial and said coefficients of said error value polynomial received from said processor, generating error locations and error values, using a linear calculation in a

Galois extension field for said input digital signals, and defining said error locations and said error values as said digital signals to be output.

Claim 14. (original) The decoding method according to claim 12, further comprising:

a i:1 multiplexing step and a 1:i demultiplexing step, wherein said input step includes the step of:

receiving said input digital signals that are Reed-Solomon codes in parallel through an i-channel.

Claim 15. (original) The decoding method according to claim 12, wherein, for optical communication, wavelength division multiplexing is used for the transmission of said input digital signals.

Claim 16. (original) The decoding method according to claim 12, wherein said input step is used for the calculation using a sequential circuit and said process step is used for the calculation using a combinational circuit.

Claim 17. (original) The decoding method according to claim 12 that is used for at least one of the correction of digital signal errors and encryption.

Claim 18. (original) A semiconductor device used to process a digital signal, said device comprising:

input means, for receiving coded digital signals;

processing means, for processing said coded digital signals and for calculating coefficients of an error locator polynomial and coefficients of an error value polynomial; and

output means, for outputting digital signals for which errors have been corrected using said coefficients of said error locator polynomial and said coefficients of said error value polynomial,

wherein said input means receives in parallel, in accordance with the number of interleaved codes, said coded digital signals, and employs said coded digital signals to calculate syndromes as data obtained serially from interleaved codes,

wherein said processing means employs said syndromes output by said input means to calculate said coefficients of said error locator polynomial and said coefficients of said error value polynomial, and

wherein said output means employs said error location, said error value and said coded input digital signals to perform an operation in a Galois

extension field, and outputs in parallel ~~the~~ obtained digital signals in accordance with said number of interleaved codes; and

wherein the processing means comprises a three stage multiplier, the three stage multiplier including an input side XOR calculator group, an AND calculator group, and an output side calculator group.

Claim 19. (original) The semiconductor device according to claim 18, further comprising:

at least one of a multiplexer and a demultiplexer, having a ratio one of i:1 and 1:i, wherein said input digital signals are Reed-Solomon codes that are received in parallel through an i-channel.

Claim 20. (original) The semiconductor device according to claim 18, wherein, for optical communication, wavelength division multiplexing is used for the transmission of said input digital signals.

Claim 21. (original) The semiconductor device according to claim 18, wherein said input means comprises a sequential circuit and said processing means comprises a combinational circuit.

Claim 22. (new) The decoding circuit of claim 1, further comprising an error correction unit configured to perform at least operations of:

inputting syndromes $S_0, \ldots S_{2t-1}$;

calculating an error locator polynomial Γ;

obtaining $\Gamma_0^{(2)}, \ldots, \Gamma_0^{(t+1)}$;

determining the maximum integer m that satisfies $\Lambda_0^{hat(m)} = \Gamma_0^{(m+1)} \neq 0$;

checking if the number of errors e is equal to the maximum number of errors;

if the number of errors is equal to the maximum number of errors, calculating an error value using $\Gamma_0^{(e+1)} = \Lambda_0^{hat(e)}, \ldots, \Gamma_e^{(e+1)}, \Gamma_0^{(e+2)} = \Lambda_0^{hat(e+1)}$;

if the number of errors is not equal to the maximum number of errors, calculating an error value using $\Gamma_0^{(e+1)} = \Lambda_0^{hat(e)}, \ldots, \Gamma_e^{(e+1)}$; and

determining $\Lambda_0^{hat(e)}, \ldots, \Lambda_e^{hat(e)}$.

Claim 23. (new) The decoder of claim 7, further comprising an error correction means configured to perform at least operations of:

inputting syndromes $S_0, \ldots S_{2t-1}$;

calculating an error locator polynomial Γ;

obtaining $\Gamma_0^{(2)}, \ldots, \Gamma_0^{(t+1)}$;

determining the maximum integer m that satisfies $\Lambda_0^{hat(m)} = \Gamma_0^{(m+1)} \neq 0$;

checking if the number of errors e is equal to the maximum number of errors;

if the number of errors is equal to the maximum number of errors, calculating an error value using $\Gamma_0^{(e+1)} = \Lambda_0^{hat(e)}, \ldots, \Gamma_e^{(e+1)}, \Gamma_0^{(e+2)} = \Lambda_0^{hat(e+1)}$;

if the number of errors is not equal to the maximum number of errors, calculating an error value using $\Gamma_0^{(e+1)} = \Lambda_0^{hat(e)}, \ldots, \Gamma_e^{(e+1)}$; and

determining $\Lambda_0^{hat(e)}, \ldots, \Lambda_e^{hat(e)}$.

Claim 24. (new) The method of claim 12, further comprising:

inputting syndromes $S_0, \ldots S_{2t-1}$;

calculating an error locator polynomial Γ;

obtaining $\Gamma_0^{(2)}, \ldots, \Gamma_0^{(t+1)}$;

determining the maximum integer m that satisfies $\Lambda_0^{hat(m)} = \Gamma_0^{(m+1)} \neq 0$;

checking if the number of errors e is equal to the maximum number of errors;

if the number of errors is equal to the maximum number of errors, calculating an error value using $\Gamma_0^{(e+1)} = \Lambda_0^{hat(e)}, \ldots, \Gamma_e^{(e+1)}, \Gamma_0^{(e+2)} = \Lambda_0^{hat(e+1)}$;

if the number of errors is not equal to the maximum number of errors, calculating an error value using $\Gamma_0^{(e+1)} = \Lambda_0^{hat(e)}, \ldots, \Gamma_e^{(e+1)}$; and

determining $\Lambda_0^{hat(e)}, \ldots, \Lambda_e^{hat(e)}$.

Claim 25. (new) The semiconductor device of claim 18, further comprising an error correction means configured to perform at least operations of:

inputting syndromes $S_0, \ldots S_{2t-1}$;

calculating an error locator polynomial Γ;

obtaining $\Gamma_0^{(2)}, \ldots, \Gamma_0^{(t+1)}$;

determining the maximum integer m that satisfies $\Lambda_0^{hat(m)} = \Gamma_0^{(m+1)} \neq 0$;

checking if the number of errors e is equal to the maximum number of errors;

if the number of errors is equal to the maximum number of errors, calculating an error value using $\Gamma_0^{(e+1)} = \Lambda_0^{hat(e)}, \ldots, \Gamma_e^{(e+1)}, \Gamma_0^{(e+2)} = \Lambda_0^{hat(e+1)}$;

if the number of errors is not equal to the maximum number of errors, calculating an error value using $\Gamma_0^{(e+1)} = \Lambda_0^{hat(c)}, \ldots, \Gamma_e^{(e+1)}$; and

determining $\Lambda_0^{hat(e)}, \ldots, \Lambda_e^{hat(e)}$.